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BAKER, STEPHEN M	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/964,195	SEKI, KATSUTOSHI	
	Examiner	Art Unit	
	Stephen M. Baker	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3-6*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: where the specification echoes the language of the claims rejected under 35 USC 112, below, corresponding amendments are necessary.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-22 are vague or misdescriptive, elliptical in some parts and prolix in other parts, not in idiomatic English, and apparently should be amended as follows:

> 1. A self orthogonal code decoding circuit for ~~performing~~ decoding ~~for~~ a self orthogonal code and repeating decoding ~~for~~ of said self orthogonal code ~~for~~ a plurality of times.
>
> 2. A self orthogonal code decoding circuit for ~~performing~~ decoding ~~for~~ a self orthogonal code on the basis of a syndrome bit determined ~~only~~ by an error in a reception series which ~~is~~ was generated ~~by adding error to~~ from a transmission series, which ~~is~~ was in turn generated by a parallel/serial conversion ~~with~~ and by adding ~~an~~ a check series to an information series, comprising:
> a plurality of decoding circuit stages ~~of deciding circuit~~ for repeating decoding ~~for~~ of said self orthogonal code ~~for~~ a plurality of times; and

a check series register output provided ~~for~~ from each ~~of~~ decoding circuit stage except ~~for the~~ from a final decoding circuit stage, ~~at a final stage among said plurality of stages of decoding circuits and~~ for inputting said check series to the next ~~stage of~~ decoding circuit stage with a delay.

3. A self orthogonal code decoding circuit as set forth in claim 2, wherein, in said plurality of decoding circuit stages ~~of decoding circuits~~, ~~a threshold value judgment~~ a reception series error detection threshold value for ~~making judgment as~~ detecting a reception series error in a first decoding stage is set ~~large to make correction~~ high for detecting a reception series error only ~~for~~ if there is a high probability of error ~~being corrected~~, and ~~said threshold value judgment~~ threshold ~~value being~~ values are gradually ~~reduced as repeated decoding for said self orthogonal code~~ lower in successive decoding circuit stages, for ~~making correction for~~ error detection when there is a lower probability of error.

4. A self orthogonal code decoding circuit as set forth in claim 2, which comprises a means for performing a code synchronization ~~judgment~~ error detection by counting the number of detected reception series errors ~~as being judged as error~~ and performing code synchronization error detection on the basis of the counted ~~error~~ number of detected errors.

5. A self orthogonal code decoding circuit as set forth in claim 3, which comprises a code synchronization dedicated ~~threshold value judgment~~ error detection circuit provided separately from ~~the~~ a circuit for ~~making judgment of~~ said reception series error detection ~~and dedicated for code synchronization and making judgment whether~~ for detecting a synchronization error ~~is caused or not~~ on the basis of ~~threshold value judgment~~ a threshold value optimized for code synchronization error detection, ~~and said threshold value of~~ said code synchronization dedicated error detection threshold value ~~judgment circuit to be~~ being lower than said ~~threshold value~~ reception series error ~~judgment~~ detection threshold value.

6. A self orthogonal code decoding circuit as set forth in claim 5, which comprises a syndrome register which shifts said syndrome bit ~~provided for code synchronization to output~~ to said code synchronization dedicated ~~threshold value judgment~~ error detection circuit, so ~~as~~ not to perform reception series error correction on the basis of the result of error ~~judgment of~~ detection by said code synchronization dedicated ~~threshold value judgment~~ error detection circuit ~~for said syndrome register~~.

7. A self orthogonal code decoding circuit as set forth in claim 4, wherein each decoding circuit in said plurality of stages comprises:

a syndrome generation means for generating said syndrome bit;

an error value generation means for ~~leading~~ generating an error value by ~~making judgment of~~ detecting an error of said syndrome bit generated by said syndrome generation means, on the basis of said reception series error detection threshold value ~~judgment threshold value~~;

an error correcting means for correcting an error of said syndrome bit on the basis of said error value generated by said error value generation means; and

an error detection counter for counting ~~said error number~~ errors on the basis of said error value generated by said error value generation means.

8. A self orthogonal code decoding circuit as set forth in claim 1, ~~wherein,~~ in a system including

an information source generating an information series,

an encoder for converting said information series into a code series, and

a communication path for transmitting said code series~~, decoding for said self orthogonal code is repeated for a plurality of times~~.

9. A self orthogonal code decoding circuit as set forth in claim 8, wherein said communication path is constructed with a wired cable.

10. A self orthogonal code decoding circuit as set forth in claim 9, wherein said wired cable is an optical cable.

11. A self orthogonal code decoding circuit as set forth in claim 8, wherein said communication path is a transmission path in radio communication.

12. A self orthogonal code decoding method for ~~performing~~ decoding ~~for~~ of a self orthogonal code and repeating decoding ~~for~~ of said self orthogonal code ~~for~~ a plurality of times.

13. A self orthogonal code decoding method for ~~performing~~ decoding ~~for~~ a self orthogonal code on the basis of a syndrome bit determined ~~only~~ by an error in a reception series which ~~is~~ was generated ~~by adding error to~~ from a transmission series which ~~is~~ was in turn generated by a parallel/serial conversion ~~with~~ and by adding ~~an~~ a check series to an information series, comprising a step of:

in each of a plurality of decoding circuit stages ~~of deciding circuit~~ for repeating decoding ~~for~~ of said self orthogonal code ~~for~~ a plurality of times, said check series ~~being~~ is input to a next decoding circuit stage ~~of decoding circuit~~ with a delay, except ~~for~~ from the ~~decoding circuit at the~~ final decoding circuit stage.

14. A self orthogonal code decoding method as set forth in claim 13, wherein, in said plurality of decoding circuit stages ~~of decoding circuits~~, a threshold value ~~judgment threshold value~~ for ~~making judgment as~~ detecting a reception series

error in a first decoding stage is set ~~large to make correction only~~ high for detecting a reception series error only ~~for~~ if there is a high probability of error ~~being corrected~~, and ~~said threshold value judgment~~ threshold ~~value being~~ values are gradually ~~reduced as repeated decoding for~~ lower in successive decoding circuit stages ~~said self orthogonal code~~, for ~~making correction for~~ error detection when there is a lower probability of error.

15. A self orthogonal code decoding method as set forth in claim 13, which comprises means for performing code synchronization ~~judgment~~ error detection by counting the number of detected reception series errors ~~as being judged as error~~ and performing code synchronization error detection on the basis of the counted ~~error~~ number of errors.

16. A self orthogonal code decoding method as set forth in claim 15, wherein a threshold value of a code synchronization dedicated ~~threshold value judgment~~ error detection circuit is provided separately from the circuit for ~~making judgment of said error~~ reception series error detection and dedicated ~~for~~ to code synchronization error detection ~~and making judgment whether error is caused or not~~ on the basis of ~~threshold value judgment~~ a threshold value optimized for code synchronization~~,~~ error detection being set lower than said reception series error detection threshold value ~~judgment threshold value~~.

17. A self orthogonal code decoding method as set forth in claim 16, which comprises a step of providing a syndrome register which shifts said syndrome bit ~~provided for code synchronization to output~~ to said code synchronization dedicated ~~threshold value judgment~~ error detection circuit, so ~~as~~ not to perform reception series error correction on the basis of the result of error detection by ~~judgment of~~ said code synchronization dedicated ~~threshold value judgment~~ error detection circuit ~~for said syndrome register~~.

18. A self orthogonal code decoding method as set forth in claim 15, which includes

~~step of~~ generating said syndrome bit,

~~step of leading~~ generating an error value by ~~making judgment of~~ detecting an error of said syndrome bit generated by said syndrome generation means on the basis of said ~~threshold value judgment~~ reception series error detection threshold value,

~~step of~~ correcting the error of said syndrome bit on the basis of said error value generated by said error value generation means;

and ~~step of~~ counting said error number on the basis of said error value generated by said error value generation means.

19. A self orthogonal code decoding method as set forth in claim 12, ~~wherein,~~ in a system including

an information source for generating an information series,
an encoder for converting said information series into a code series, and
a communication path for transmitting said code series~~, decoding for said self orthogonal code is repeated for a plurality of times~~.

20. A self orthogonal code decoding method as set forth in claim 19, wherein said communication path is constructed with a wired cable.

21. A self orthogonal code decoding method as set forth in claim 20, wherein said wired cable is an optical cable.

22. A self orthogonal code decoding method as set forth in claim 19, wherein said communication ~~oath~~ path is a transmission path in radio communication.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 2, 8, 11-13, 19 and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. patent No. 6,167,552 to Gagnon et al (hereafter referred to as Gagnon).

Gagnon discloses a channel coding decoder (Fig. 2) for recovering data from noisy channels by repeatedly decoding a convolutional "self orthogonal code", in a plurality of decoding circuit stages (26). Iterative decoding with Gagnon's channel code and decoder is presumably much faster than iteratively decoding appreciably interleaved channel coding arrangements.

Regarding claims 11 and 19, Gagnon specifically mentions telephone and satellite wireless channels for a applications of the coding and decoding.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gagnon.

Gagnon (Fig. 3) shows a decoder stage (26), including a shift register for delaying the parity bits (S). Gagnon does not clearly show omitting the parity bit output line from the connected output lines form the final decoder stage. It would have been obvious to a person having ordinary skill in the art to leave the parity output line of Gagnon's convolutional parity decoder's last stage disconnected because there is of course no need for the parity bits after parity decoding is complete.

7. Claims 9, 10, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gagnon in view of the published article by Yuan (hereafter referred to as Yuan).

Gagnon doesn't specifically mention wire and optical cables as applicable noisy media.

The error correcting advantages of using convolutional coding on wire and optical cables was well known at the time the invention was made, as it was also well known that increasingly filling out the bandwidth capacities of wire and optical cables, such as by using multi-carrier techniques including WDM and OFDM, calls for stronger error correction. The error correcting usefulness of self-orthogonal convolutional codes on optical cables was also well known at the time the invention was made, as shown by Yuan, for example.

It would have been obvious to a person having ordinary skill in the art to apply Gagnon's convolutional channel coding system to error correction for wire and optical cable channels. Such an application would have been obvious because the error correcting usefulness of self-orthogonal convolutional codes on optical cables was already well known, as shown by Yuan.

8. Claims 4 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gagnon in view of U.S. Patent No. 3,806,647 to Dohne *et al* (hereafter referred to as Dohne).

Gagnon doesn't teach counting errors for synchronization correction control.

The advantages of correcting synchronization errors using counted bit error detections from a convolutional code decoder was well known at the time the invention was made, as shown by Dohne, for example.

It would have been obvious to a person having ordinary skill in the art to apply counted bit error detections from Gagnon's convolutional channel coding system to synchronization error correction, as has been similarly done with Dohne's convolutional

channel coding system. Such an application would have been obvious because the usefulness of synchronization error correction by counting bit error detections from a convolutional code decoder was already well known, as shown by Dohne.

Allowable Subject Matter

9. Claims 2, 3, 5-7, 13, 14 and 16-18 would be allowable if rewritten to overcome the rejections under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen M. Baker whose telephone number is (703) 305-9681. The examiner can normally be reached on Monday-Friday (11:00 AM - 7:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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smb